UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/054,933	04/03/1998	CRAIG R. FRINK	A0521/7153	3289

26643 7590 10/07/2002

PETER J. GORDON, PATENT COUNSEL
AVID TECHNOLOGY, INC.
ONE PARK WEST
TEWKSBURY, MA 01876

EXAMINER	
BUI, KIEU OANH T	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/054,933	FRINK, CRAIG R.	
	Examiner	Art Unit	
	KIEU-OANH T BUI	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durana et al. (U.S. Patent No. 6,018,765) in view of Favor (U.S. Patent No. 5,819,056).

Regarding claim 1, Durana et al. (or "Durana" hereinafter) discloses an output interface for a sender of video data having an output for providing video data, i.e., video data is provided to users or the system including an output interface such as video and audio outputs (Fig. 6 and col. 8/lines 16-27) for providing video data (col. 1/line 55 to col. 2/line 4); wherein the output interface transfers data and asserts one of the valid data signal and the valid command signal to the receiver in response to a request signal received from the receiver, i.e., valid data signal including the valid command signal are transferred by the output interface to the receiver or the viewer (Fig. 2/at the set-tops 42) in response to a request signal from the receiver, for instance, as the viewer sends a request signal for selecting a program by pushing a preselected button on his/her set-top box or a remote control (col. 4/lines 4-21).

Durana does not teach the steps of comprising "a valid data signal associated with the data indicating whether the associated data includes valid video data; and a valid command signal indicating whether the data includes command data; and wherein the command data includes a memory address at a receiver of the data"; however, Favor teaches a computer system wherein the command or control data can be checked whether valid or not by an execution engine in including an instruction decoder for tracking and monitoring the command data including the memory address at the receiver, i.e, which is a memory 130 in this scenario (see Fig. 2, and col. 32/lines 11-39 & col. 33/lines 28-40 & Fig. 9 and col. 36/line 46 to col. 37/line 40 for details on the procedure on read & write instructions for decoding valid signals). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Durana's technique with Favor's teaching technique of decoding valid signals using instructions to verify memory addresses at the receiver in order to provide valid data signals including valid command signal in response to a request signal at the receiver.

Regarding claim 2, Durana discloses an input interface for a receiver of video data having an input for receiving data, i.e., input interface of the decoder in this configuration having input for receiving data from the host (Fig. 3/item 14, and col. 1/line 55-col. 2/line 4); wherein the input interface transfers video data received to the memory address specified in the command data in the memory of the receiver (as illustrated in Figs. 10 & 12, and col. 13/lines 12-20 & col. 16/lines 16-36 for a specified memory address as brought up by the command data, which provides an allocation memory address table for the receiver to perform).

Durana does not address the steps of comprising "a valid data signal associated with the data indicating whether the associated data includes valid video data; and a valid command signal indicating whether the data includes command data; and wherein the command data includes a memory address at a receiver of the data"; however, Favor teaches a computer system wherein the command or control data can be checked whether valid or not by an execution

engine in including an instruction decoder for tracking and monitoring the command data including the memory address at the receiver, i.e, which is a memory 130 in this scenario (see Fig. 2, and col. 32/lines 11-39 & col. 33/lines 28-40 & Fig. 9 and col. 36/line 46 to col. 37/line 40 for details on the procedure on read & write instructions for decoding valid signals). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Durana's tecnique with Favor's teaching technique of decoding valid signals using instructions to verify memory addresses at the receiver in order to provide valid data signals including valid command signal in response to a request signal at the receiver.

Regarding claim 3, Durana and Favor teach a device for reading video data from a memory in another device, i.e., a multimedia server (as illustrated in Durana - Fig. 2/item 30), comprising: an output interface having an output for providing data, and a valid data signal associated with the data indicating whether the associated data is valid video data, and a valid command signal indicating whether the data includes command data, and wherein the command data includes a memory address in the memory in the other device, and having an input for receiving a request signal from the other device; wherein the output interface transfers data to the other device in response to a request signal received from the other device (see the Examiner's discussion in claim 1 above); and an input interface having an input for receiving data, and a valid data signal associated with the data indicating whether the associated data is valid video data (see Examiner's discussion in claim 2 above).

As for claim 4, in further view of claim 3 above, Durana and Favor further disclose a memory, i.e., a mass storage for storing a plurality of video data files (Durana - Fig. 3/item 12, and col. 4/lines 31-44 & col. 6/lines 10-23); and wherein the input of the input interface further receives a valid command signal indicating whether the data includes command data, wherein the command data includes a memory address in the memory of the device, wherein the input

interface transfers valid data received to the memory address specified in the command data in the memory of the device (see Examiner's discussion in claim 2 above).

As for claim 5, in further view of claim 3 above, Durana and Favor further disclose a queue of memory addresses sent in command data to the other device, i.e., stream of data sent to a first in first out memory (FIFO) in providing a read/write storage to buffer data transferred over the system bus (Fig. 9, and col. 11/line 40-col. 12/line 13) which including memory addresses conveyed in the command data (col. 13/line 54 to col. 14/line 26); and wherein the input of the input interface further receives a valid command signal indicating whether the data includes command data, i.e., a valid command data is supplied by the host in transferring those valid data (col. 5/line 55 to col. 6/line 9); wherein the command data includes a memory address in the memory of the other device, wherein the input interface determines whether the memory address corresponds to a memory address in the queue, i.e., the command data comprises a full set of functions which allows the viewer to control a program (col. 5/lines 55-67) which also including a memory address or memory allocation table for the host to send appropriate requested data (Fig. 10, and col. 13/lines 12-20 & col. 16/lines 16-36 for more details on a memory map) as well as an illustration in Figure 12 for memory address of the other device therein.

Regarding claims 6-8, Durana and Favor disclose "a device for providing video data to another device, comprising: a memory for storing video data; an input interface having an input for receiving data, and a valid command signal indicating whether the data includes command data, wherein the command data includes a memory address in the device, wherein the input interface reads video data from the memory in the device using the memory address specified in the command data; an output interface having an output for providing data, and a valid data signal associated with the data indicating whether the associated data is valid video data; wherein the output interface transfers the video data read from the memory to the other device in response to a request signal received from the other device"; "wherein the input of the input interface

further receives a valid data signal indicating whether the data includes valid video data, wherein the input interface transfers valid data received to the memory address specified in the command data in the memory of the device"; and further "comprising a queue of memory addresses received in command data from the other device; and wherein the output of the output interface further sends a valid command signal indicating whether the data includes command data, wherein the command data includes a memory address in the memory of the device, wherein the input interface outputs a memory address from where the data was read" (see claims 1 and 3-5 above).

Regarding claim 9, Durana and Favor teaches a device for receiving video data from another device, i.e., a decoder for receiving video data from the host (Durana - Fig. 2/item 14) comprising: a memory for storing the video data, i.e., a mass storage for storing a plurality of video data files (Durana - Fig. 3/item 12, and col. 4/lines 31-44 & col. 6/lines 10-23); an input interface having an input for receiving data, i.e., input interface of the decoder in this configuration having input for receiving data from the host (Durana - Fig. 3/item 14, and col. 1/line 55-col. 2/line 4); and a valid data signal indicating whether the data includes valid video data, i.e., a programmable logical device (PLD) control data transfers (Durana - Fig. 9/item 222, and col. 14/lines 28-38), under the control of this PLD inputs and outputs device, the status of data, whether it is a valid video data or not, can be determined based on their memory addresses (see col. 16/lines 37-66); and a valid command signal indicating whether the data includes command data, i.e., a valid command data is supplied by the host in transferring those valid data (col. 5/line 55 to col. 6/line 9); wherein the command data includes a memory address in the device, i.e., the command data comprises a full set of functions which allows the viewer to control a program (col. 5/lines 55-67) which also including a memory address or memory allocation table for the host to send appropriate requested data (Fig. 10, and col. 13/lines 12-20 & col. 16/lines 16-36 for more details on a memory map); wherein the input interface stores video

data received from the other device in the memory in the device at the memory address specified in the command data (as illustrated in Figs. 10 & 12, and col. 13/lines 12-20 & col. 16/lines 16-36 for a specified memory address as brought up by the command data, which provides an allocation memory address table for the receiver to perform); an output interface having an output for providing a request signal, wherein the other device transfers the video data to the device in response to the request signal, i.e., valid data signal including the valid command signal are transferred by the output interface as mentioned above to the receiver or the viewer (Fig. 2/at the set-tops 42) in response to a request signal from the receiver, for instance, as the viewer sends a request signal for selecting a program by pushing a preselected button on his/her set-top box or a remote control (col. 4/lines 4-21; and the Examiner's dicussion in claims 1-2 above).

As for claim 10, Durana and Favor teach "a device for writing video data to a memory in another device, comprising: an output interface having an output for providing data, and a valid data signal associated with the data indicating whether the associated data is valid video data, and a valid command signal indicating whether the data includes command data, and wherein the command data includes a memory address in the memory in the other device, and having an input for receiving a request signal from the other device; wherein the output interface transfers data to the other device in response to a request signal received from the other device" (see Examiner's discussion in claim 6 above).

Conclusion

4. The prior art made of record and not replied upon is considered pertinent to applicant's disclosure.

Favor et al. (U.S Pat. No.6,093,213) disclose a flexible implementation of a system management mode (SMM) in a processor.

Bonke et al. (U.S. Pat. No.5,661,848) disclose a multiple-drive data-storage system include a multiple-drive controller.

Bleidt et al. (U.S. Pat. No.5,920,702) disclose a method of stripping a data stream onto subsets of storage devices in a multiple user data distribution system.

5. **Any response to this action should be mailed to:**
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:
(703) 872-9314, (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista Kieu-Oanh Bui whose telephone number is (703) 305-0095. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM, with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile, can be reached on (703) 305-4380.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

ANDREW FAILE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Krista Bui
Art Unit 2611
September 26, 2002